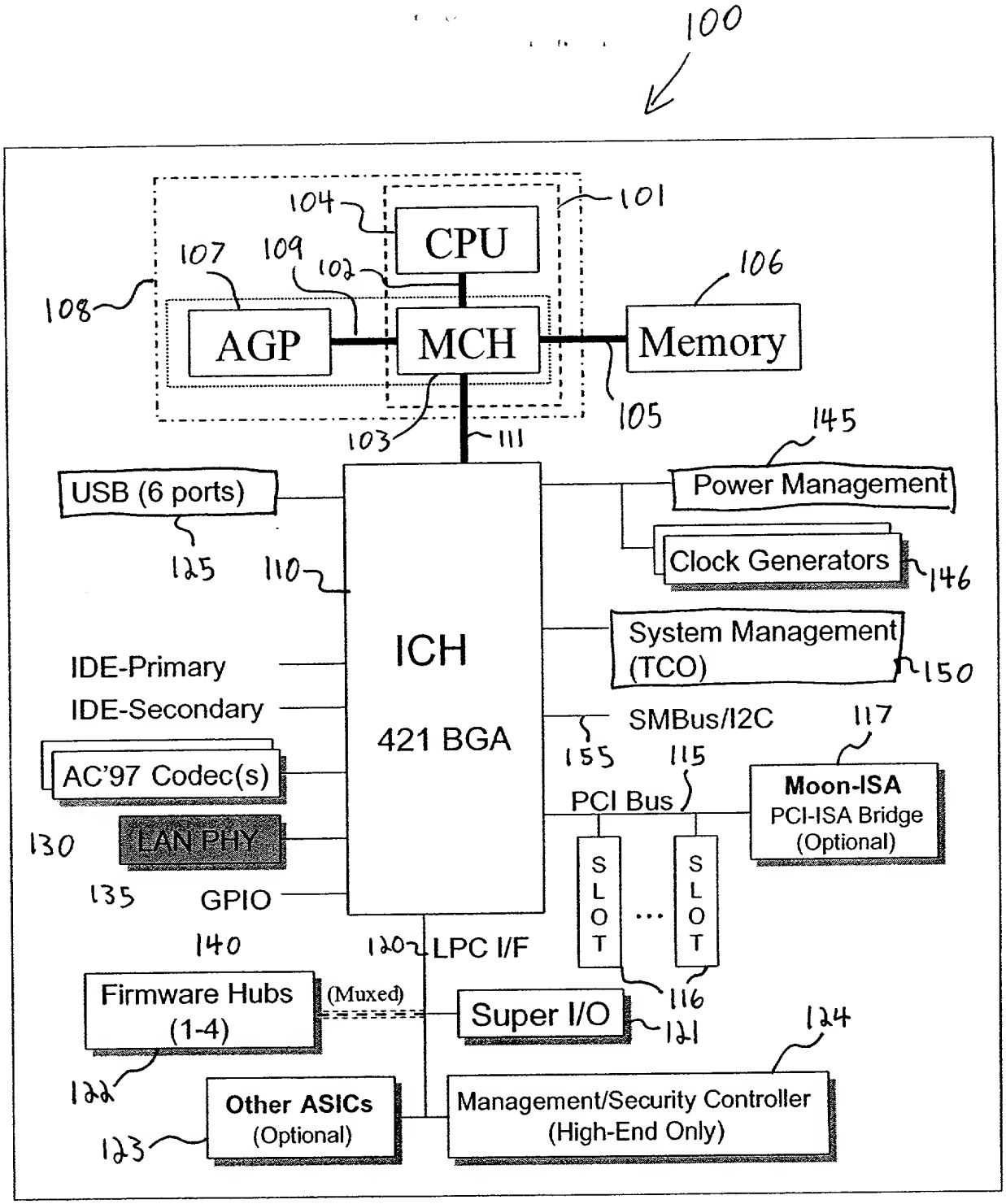

Figure 1. Desktop System Diagram

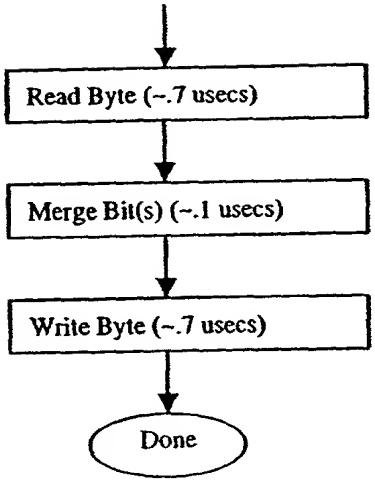

Fig. 2

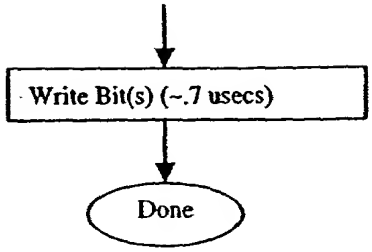

Fig. 4

	Bit Enables				Register Bits				Comments
	3	2	1	0	3	2	1	0	
Initial Value					0	0	1	1	
Software Write "1010_1X0Xb"	1	0	1	0	1	X	0	X	Bits 3 and 1 are enabled to be overwritten
Resulting Value					1	0	0	1	Bits 3 and 1 are overwritten, while bits 2 and 0 retain their initial values

Fig. 3

500

Address storage device so as to command the attention of storage device

502

Read an alt-status register of storage device to determine whether storage device 2 is busy.

504

If storage device is busy, then return a "SRB_STATUS_BUSY" signal.

506

If storage device is not busy, determine whether the BM is active.

508

If the BM engine is active, then the BM engine may be turned off and the drive reset.

510

If the BM engine is not active, then calculate the block count and the program device.

512

514

Calculate the logical block address (LBA) and the program device.

Programming up the direct memory access (DMA) descriptor table contents.

The command register may be programmed with a read or write command.

The DMA engine may be programmed.

Wait for an interrupt signal.

Receive an interrupt signal.

524

Fig. 5

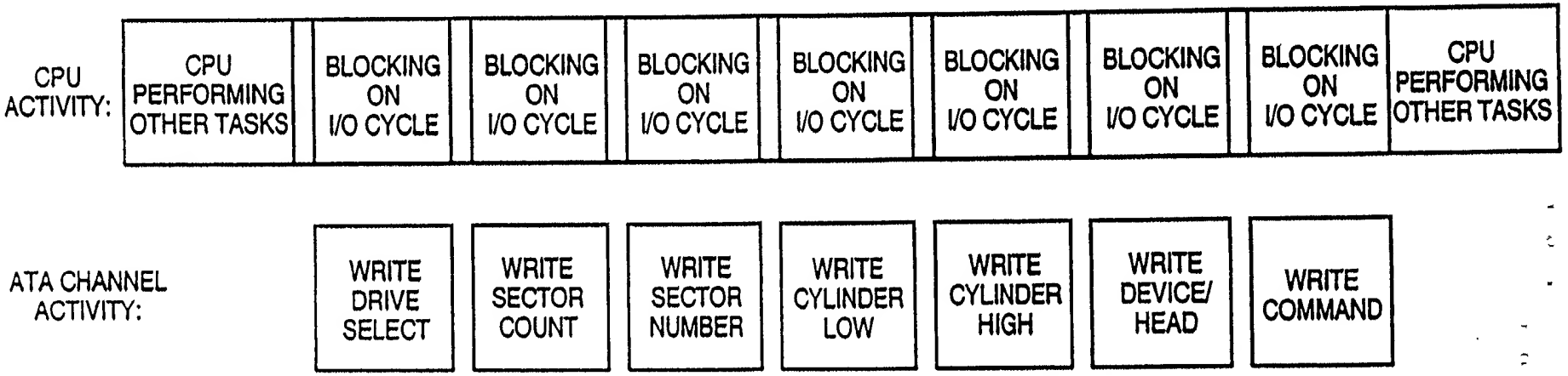

Fig. 6

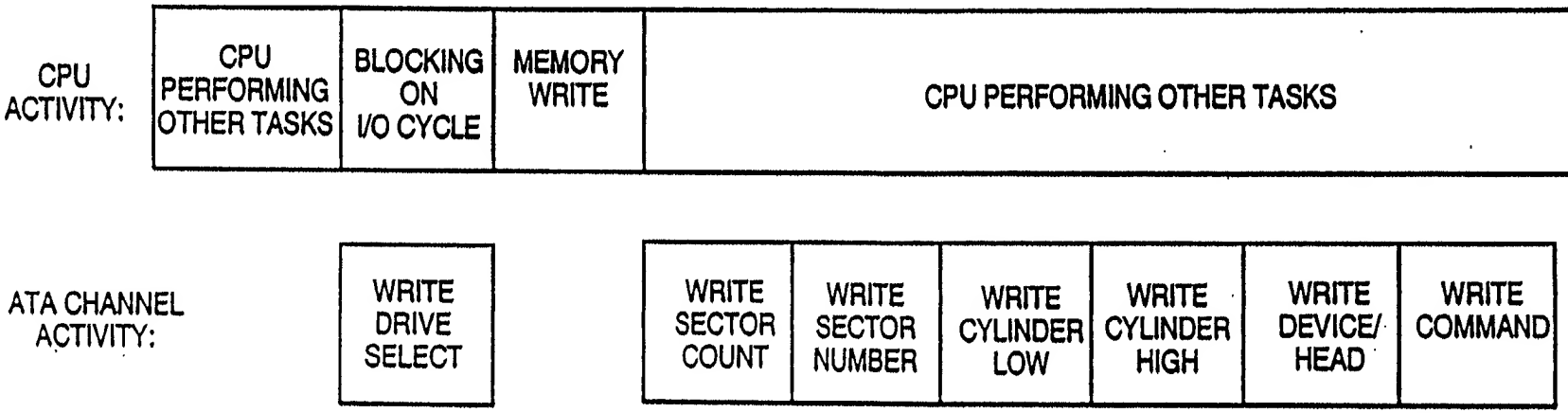

Fig. 7